LPP EUV Source Production for HVM

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CYMER
Leading the Light Generation.

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Introduction

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Progress and Status Summary

- Total of eight HVM I sources built and operational
  - Four sources installed and exposing wafers at customer sites
  - Installation of a fifth source at user site is in process
  - Field teams in place to support 24x7 operation globally
  - One HVM I source installed at ASML for NXE:3100 scanner development
  - Two remain in San Diego for upgrade development and reliability enhancements
  - Availability of sources in field approximately 50% (SEMI E10 definition)
  - Power upgrade to 8W released and in process of being installed at Fabs
- HVM I Power Upgrades
  - Demonstrated 35W expose power at high duty cycle on HVM I source
  - Demonstrated 100W expose power at low duty cycle with pre-pulse on LT1
- HVM II source hardware program
  - Program schedule on track for February first light
  - 28kW CO_2 laser power demonstrated to support NXE:3300 initial power target

Cymer EUV Operations in San Diego

Corporate Headquarters
(CSD4 – 130,000 ft^2)

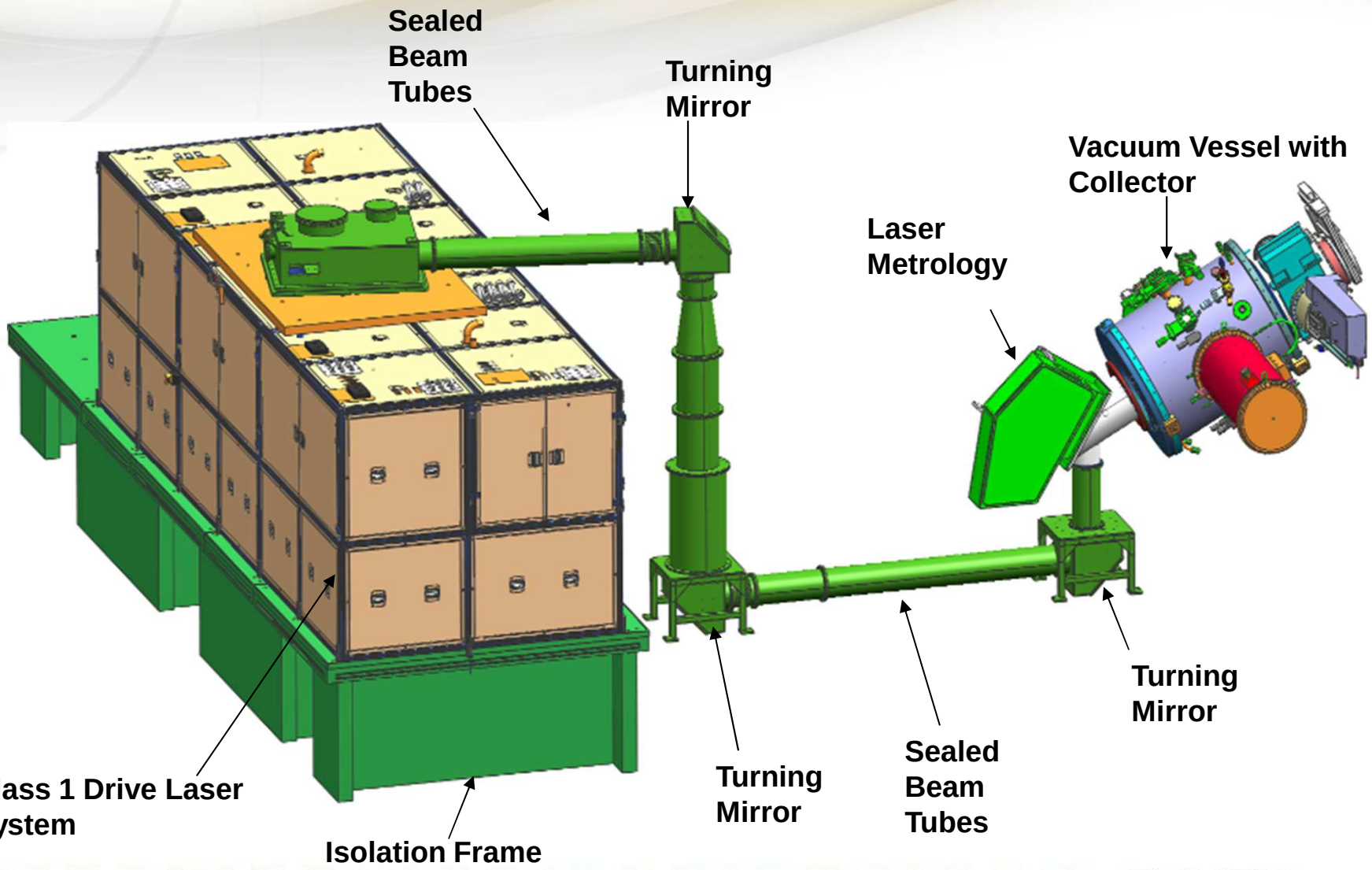
- **EUV Operations**
  - R&D (6000 ft^2)
  - Marketing and Management

Manufacturing Facility
(CSD6 – 265,000 ft^2)

- **EUV Operations**
  - Engineering and Manufacturing (32,000 ft^2)
    - Capacity for 1 source per month by mid 2012
  - Service and support

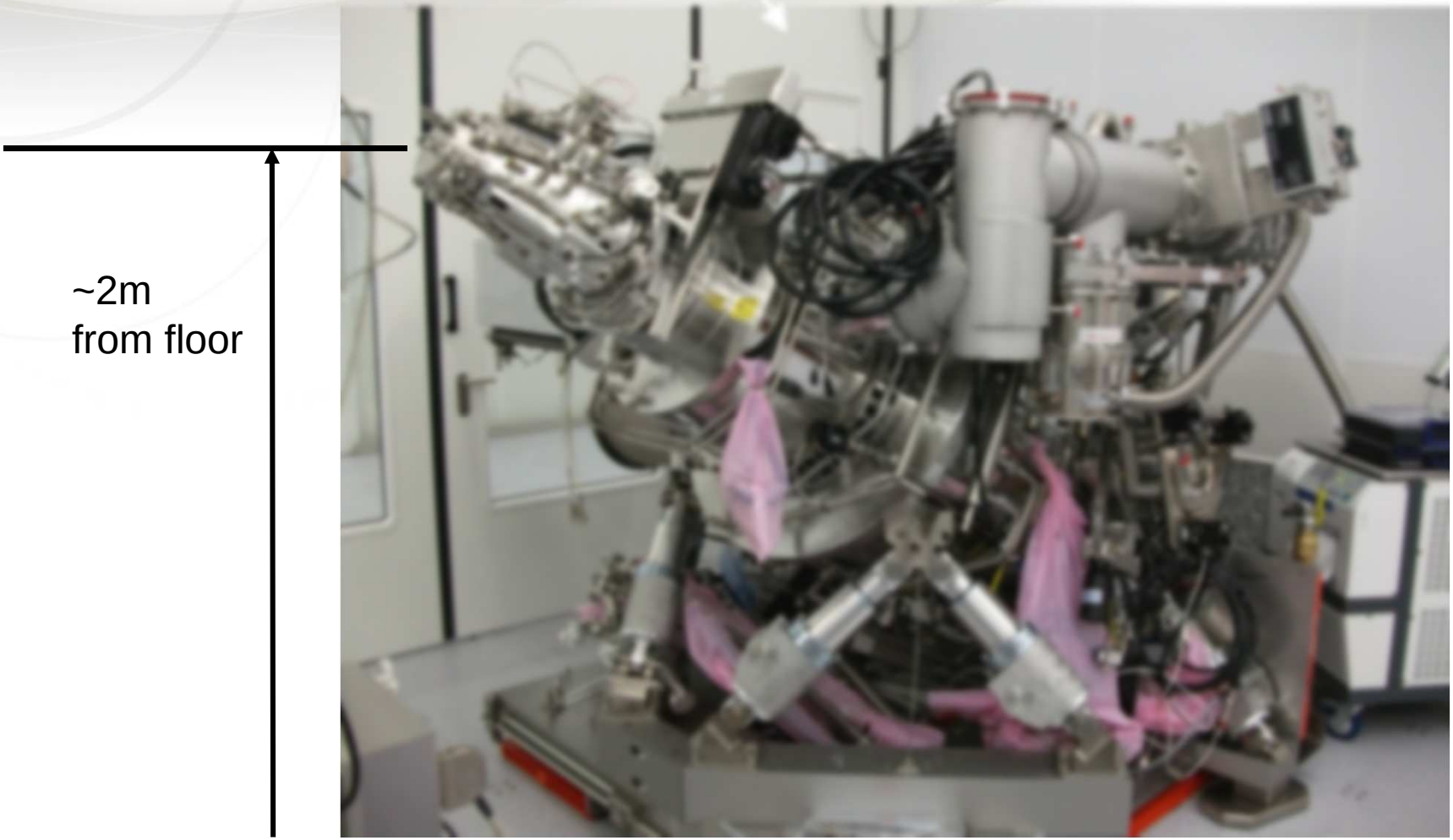
HVM I Laser Produced Plasma EUV Source

Schematic Layout Shown for Single Floor



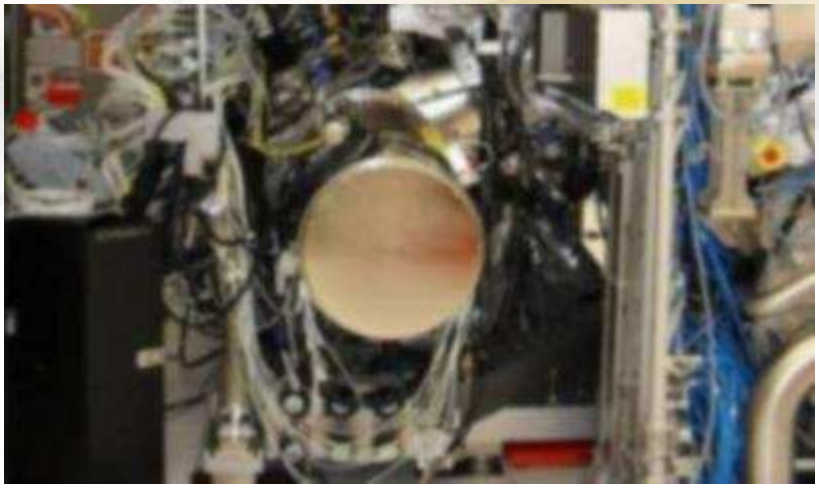
HVM I Source Vessel Fully Populated

HVM I source in the cleanroom at ASML



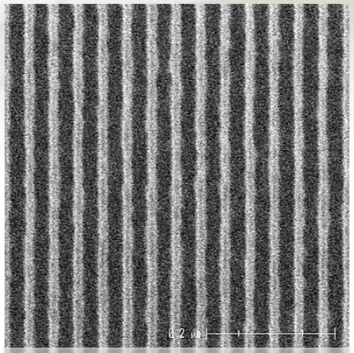
Cymer LPP Source Integrated into ASML NXE:3100

Supporting 7 days/wk x 24 hrs/day operations in all locations

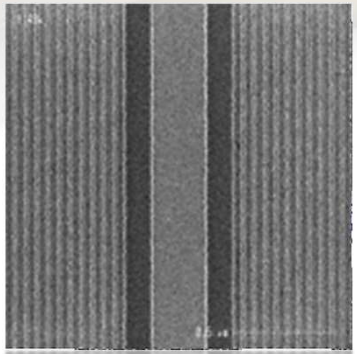


Imaging Performance with LPP Sources on NXE:3100

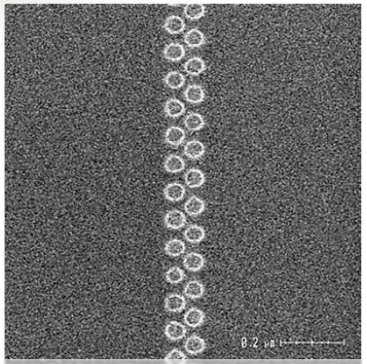
Enabling EUV Lithography



19 nm dense lines

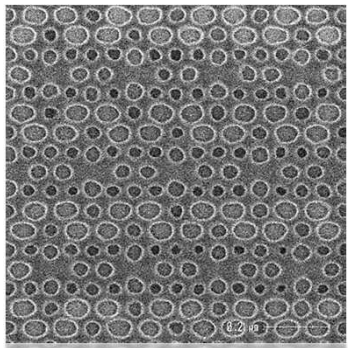


27 nm Gate Layer Flash



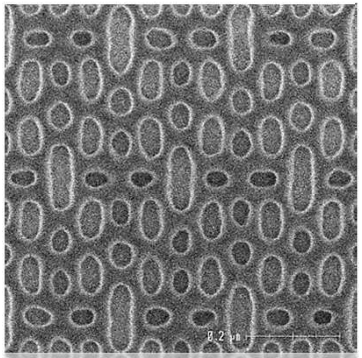
Flash staggered contact layer

Bitline pitch = 44 nm (1:1.2)
CH pitch = 74.4 nm



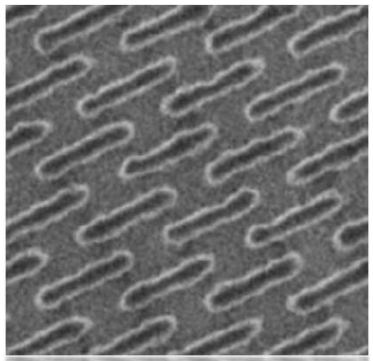
Sub 16 nm node SRAM Contact Hole

0.038µm2 bit cell-size,
hp 30/32 nm



Sub 16 nm node SRAM metal-1

0.038µm2 bit cell-size,
hp 30/32 nm



30 nm Brickwall DRAM

Courtesy of ASML

Worldwide Cymer LPP Source Installed Base

Location	Status	Description
HVM I Sources		
Chipmaker	Device development	Installed and operational, since Dec 2010
Chipmaker	Device development	Installed and operational, since March 11’
Chipmaker	Qualification test	Shipped to ASML in August 10’, user installation in process
Chipmaker	Qualification test	Direct ship to end user from Cymer
Chipmaker	Installation	Shipped to ASML in April 10’, user installation in process
ASML	Installation	To be used for scanner development at ASML
Cymer Internal	Upgrade 2 (Pre-pulse)	Pre-pulse hardware installed and testing is underway, June ‘11 demonstration of 30W 80% duty cycle and 25W/100% duty cycle
Cymer Internal	Upgrade 0.5 and 1.0, and collector life-testing	Demonstrated 11W average expose power >100 hour Improved coating lifetime testing
HVM II Sources		
Cymer→ASML	Build process started	Early source to support 3300 program
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Cymer Internal	Procurement	RD&E source for 3300 development
Cymer Internal	Procurement	RD&E source for 3300 development
Cymer→ASML	Procurement	First full 3300 integration source
Cymer→ASML	Procurement	3300 integration source
Additional HVM II sources planned committed for delivery 2012-2013		

HVM I Performance

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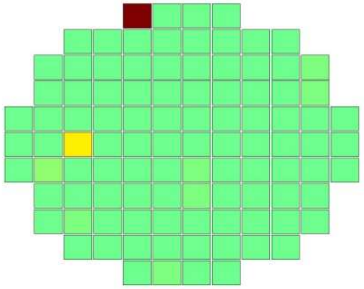
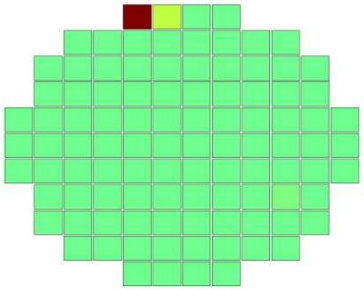
Current HVM I Performance

- 8W average exposure power at 60% duty cycle is qualified by Cymer and released to the field for upgrade
- <1.0% dose stability on >90% of fields, exceeded interim target
- Automation is complete for dose control, and plasma position control in three dimensions (x, y, z)
- Machine software is complete to eliminate operator intervention (expect an increase in availability of >10%)
- ~50% Availability (SEMI E10 Definition)
  - Other 50% of time is used for maintenance, primarily on two modules; Droplet Generator and Collector

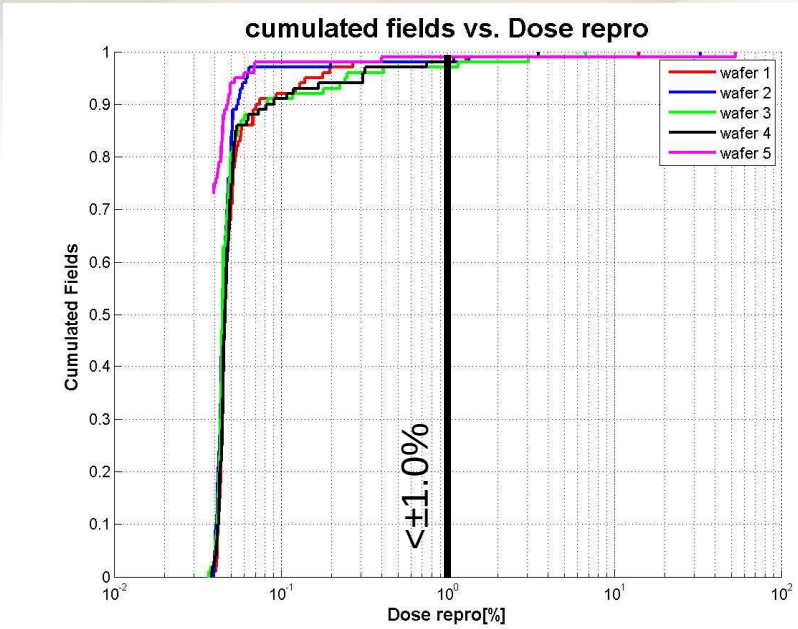
8W Average Exposure Power Demonstration over 8 hours on HVM I Source at 60% Duty Cycle



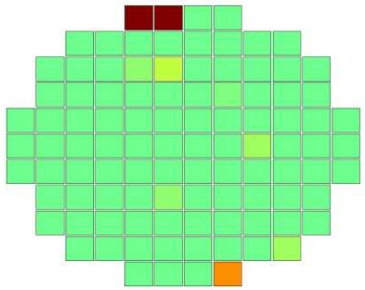
WAFER 1



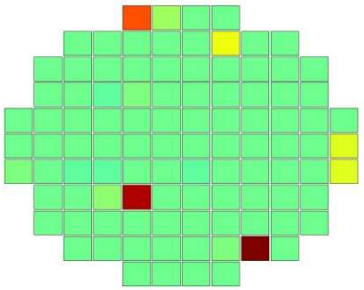
WAFER 2



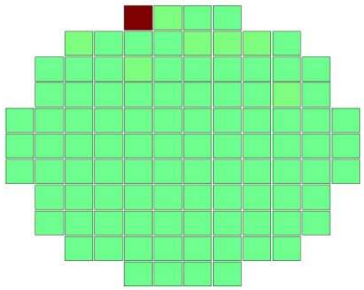
- Seven lots of 5 wafers each with 100 fields per wafer at 8W average power all meeting interim dose stability target



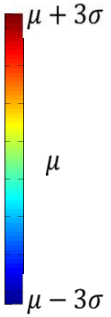
WAFER 3



WAFER 4

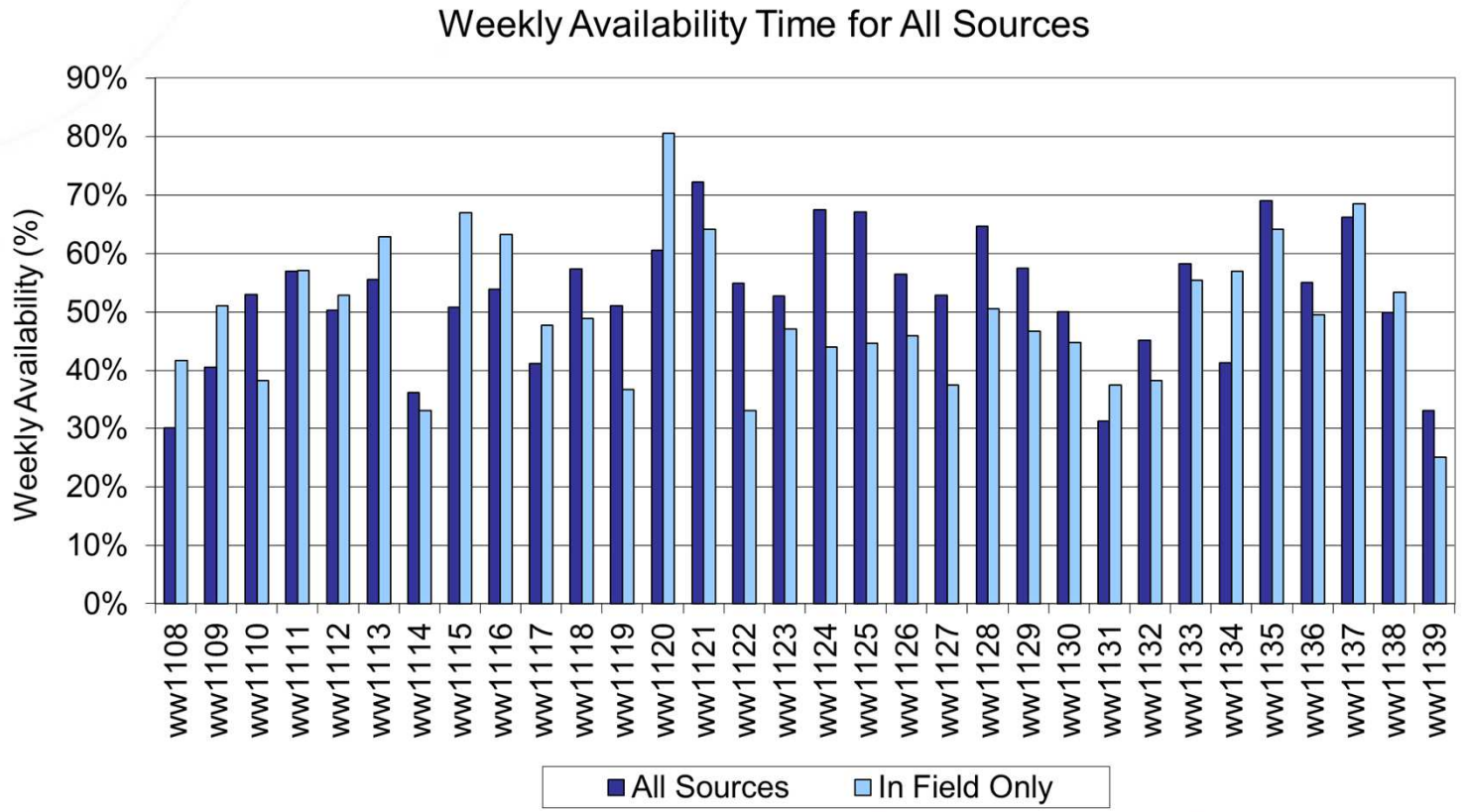


WAFER 5



HVM I Source Availability Year-to-Date

	1Q2011	2Q2011	3Q2011	4Q2011
Target	35%	40%	53%	61%
All Sources	48%	55%	52%	
In Field Only	51%	50%	48%	



HVM I Roadmap and Upgrades

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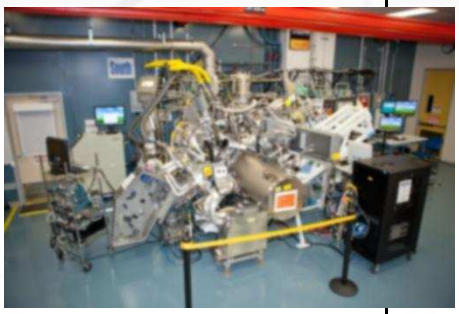
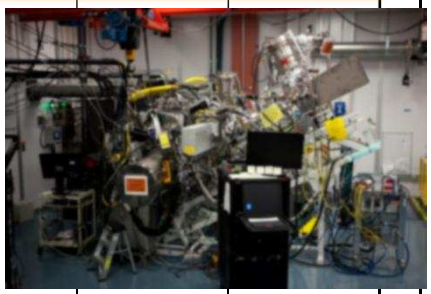
HVM I Source – Near Term Power Upgrade Roadmap



Dedicated test source for Upgrades 2a and 2b

Upgrade 2b
- 100W Ave. Exposure Power
- <0.2% Dose Stability
- Continuous mode with prepulse

Upgrade 2a
- 50W Ave. Exposure Power
- <0.2% Dose Stability
- Continuous mode



Dedicated test source for Upgrade 1

Upgrade 1
- 20W Ave. Expose Power
- <0.5% Dose Stability
- Burst mode, 90% duty cycle

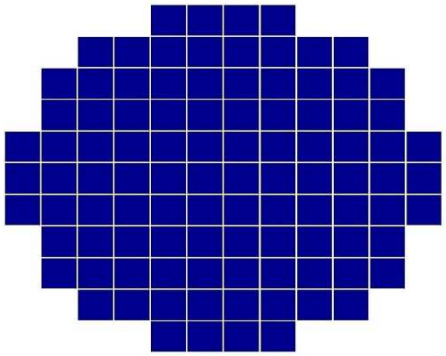
Q4 2011			Q1 2012			Q2 2012		
Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun

Q4 2011			Q1 2012			Q2 2012		
Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun

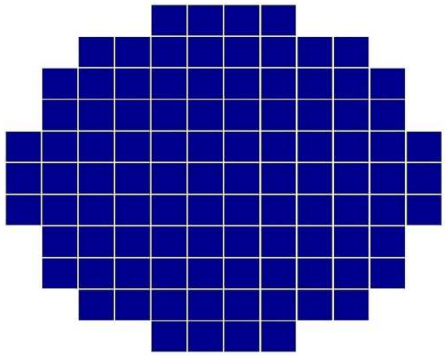
qualified

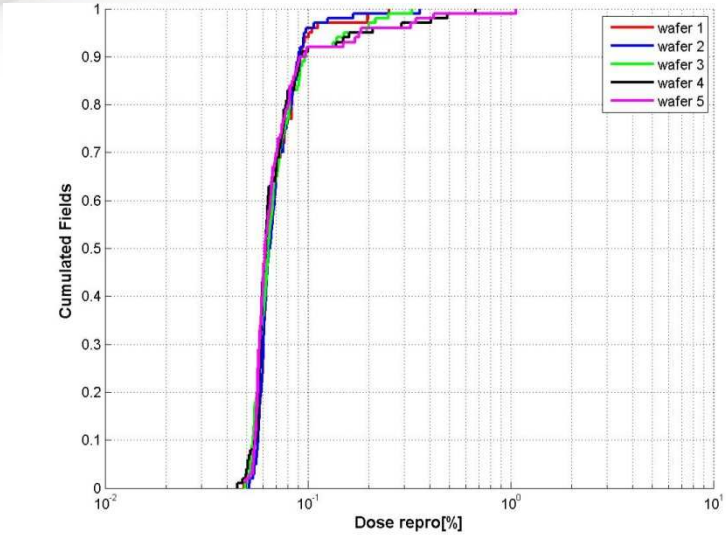
Upgrade 1: ~15W Average Exposure Power at 90% Duty Cycle Dose Stability by Die over Five Wafers

WAFER 1

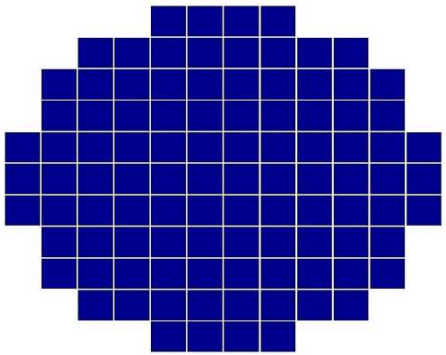


WAFER 2

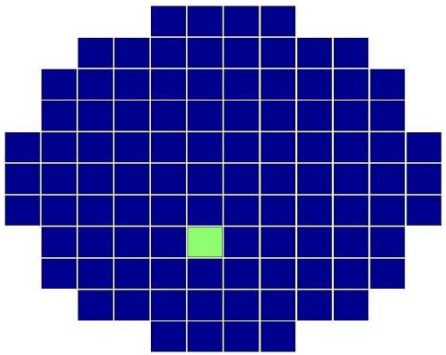




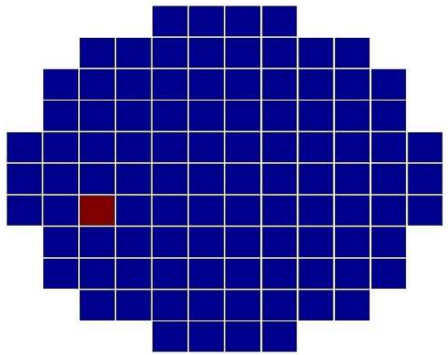
WAFER 3



WAFER 4



WAFER 5

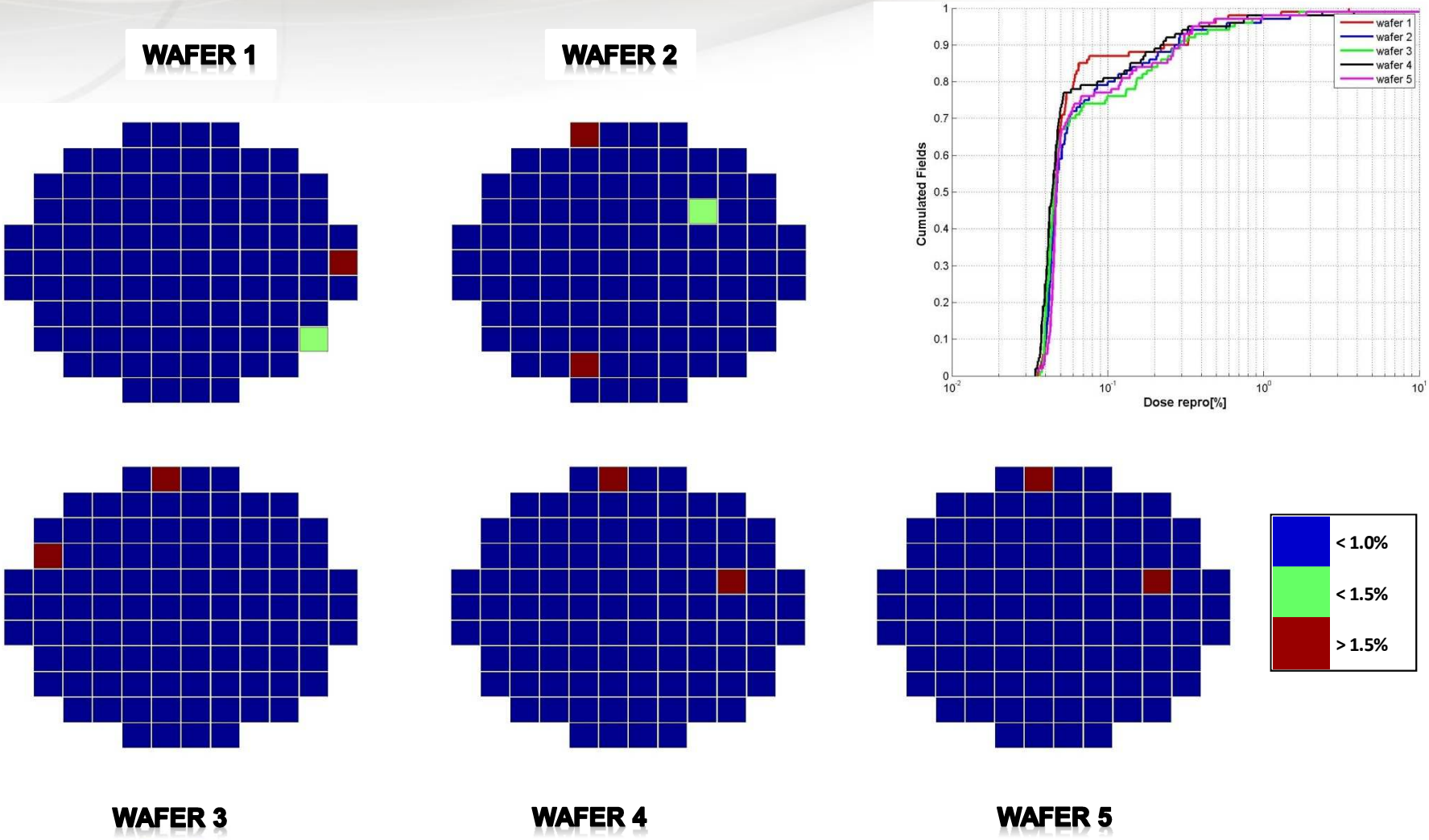


< 0.5%

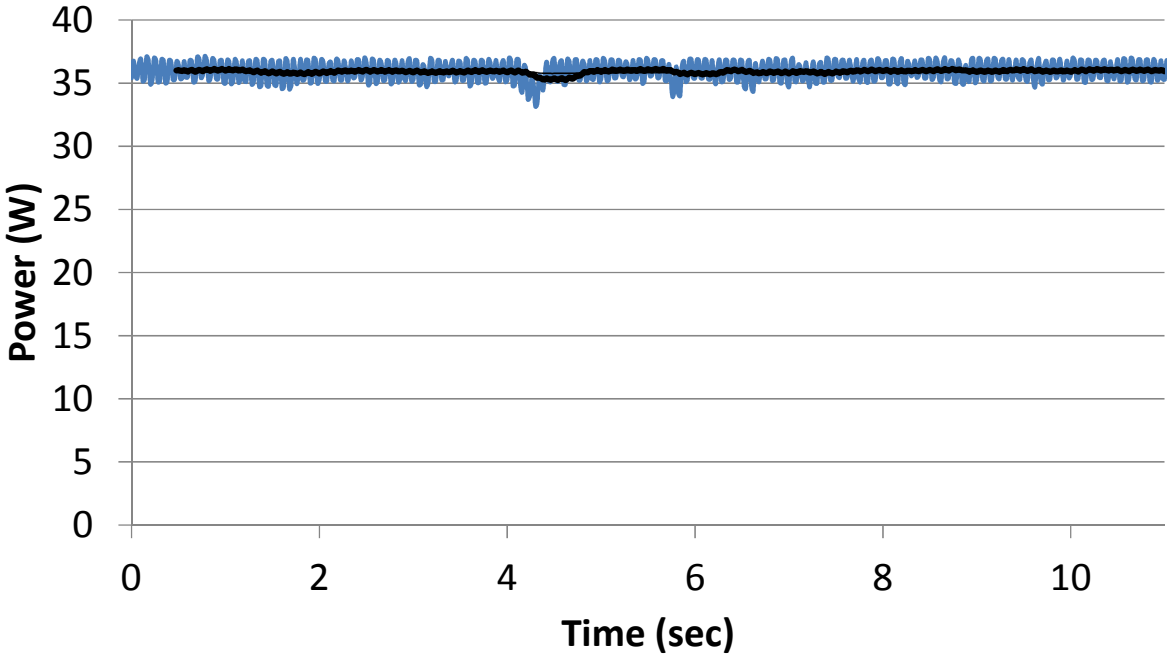
< 1.0%

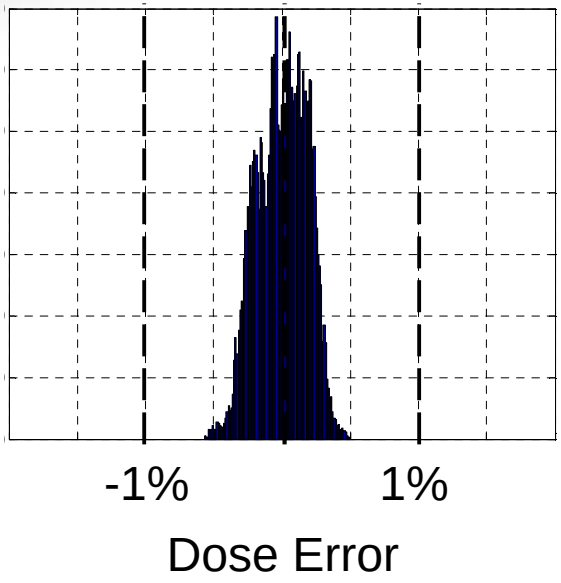
> 1.0%

Upgrade 1: ~19W Average Exposure Power at 90% Duty Cycle Dose Stability by Die over Five Wafers

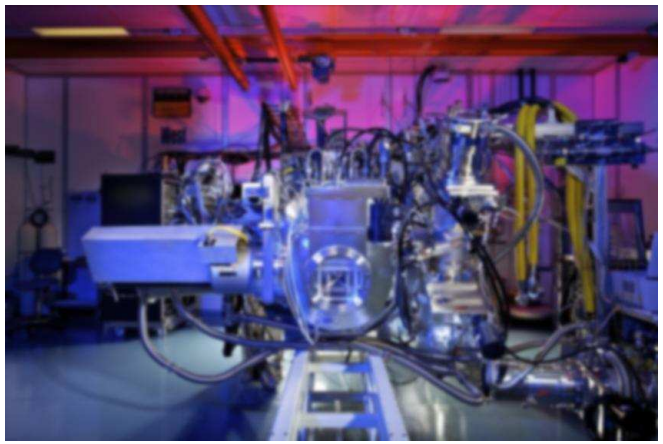


Upgrade 2a: ~35W Average Exposure Power at High Duty Cycle on an HVM I Source

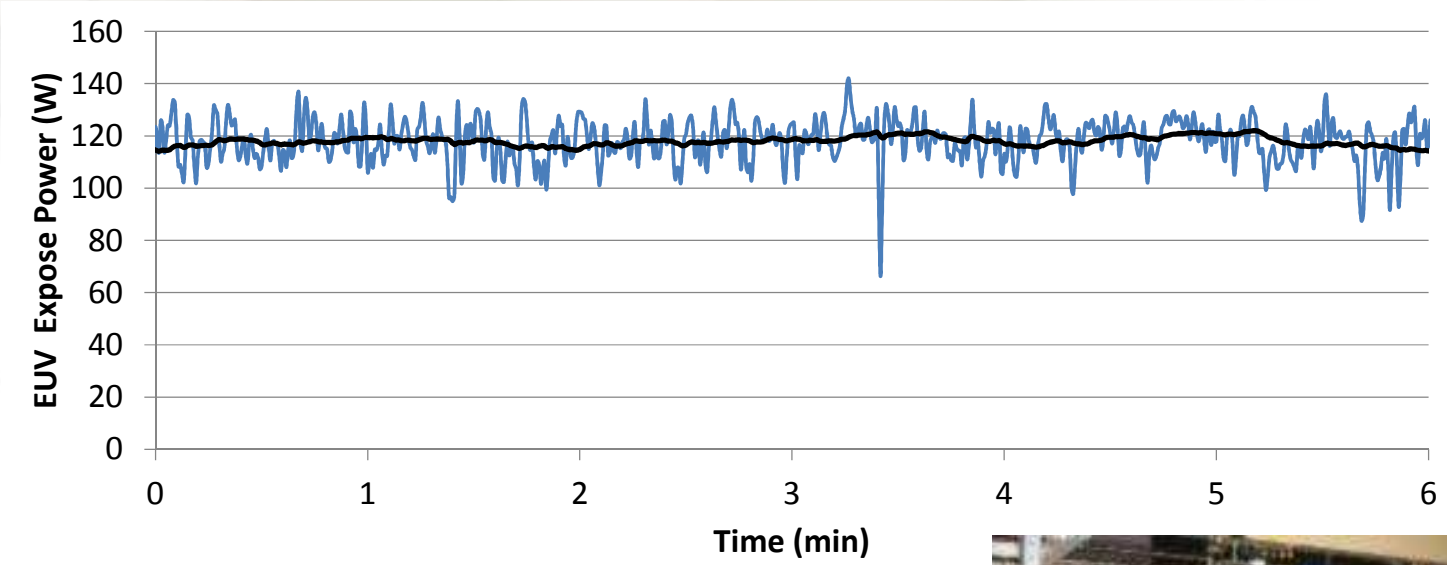




- 80% Duty Cycle
- <±0.5% Dose Stability
- Feasibility at low duty cycle (LT1) supports 50W target
  - Laser upgrade to LT1 configuration ongoing



>100W Power Demonstration at Low Duty Cycle with Prepulse on LT1

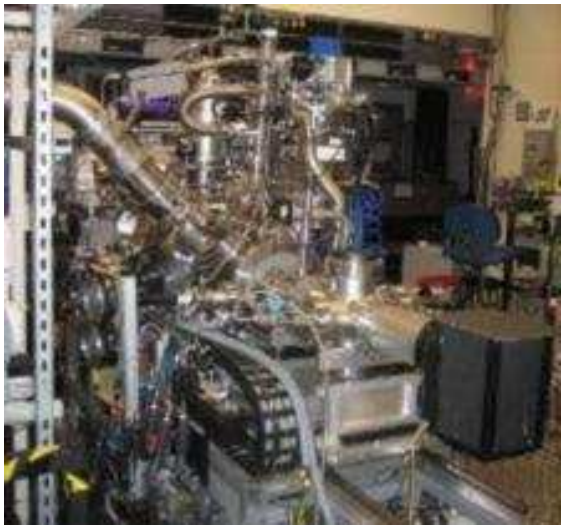


LT1

- >100W Calculated Exposure Power
- ~20kW CO_2 Laser Power
- Low duty cycle / no collector

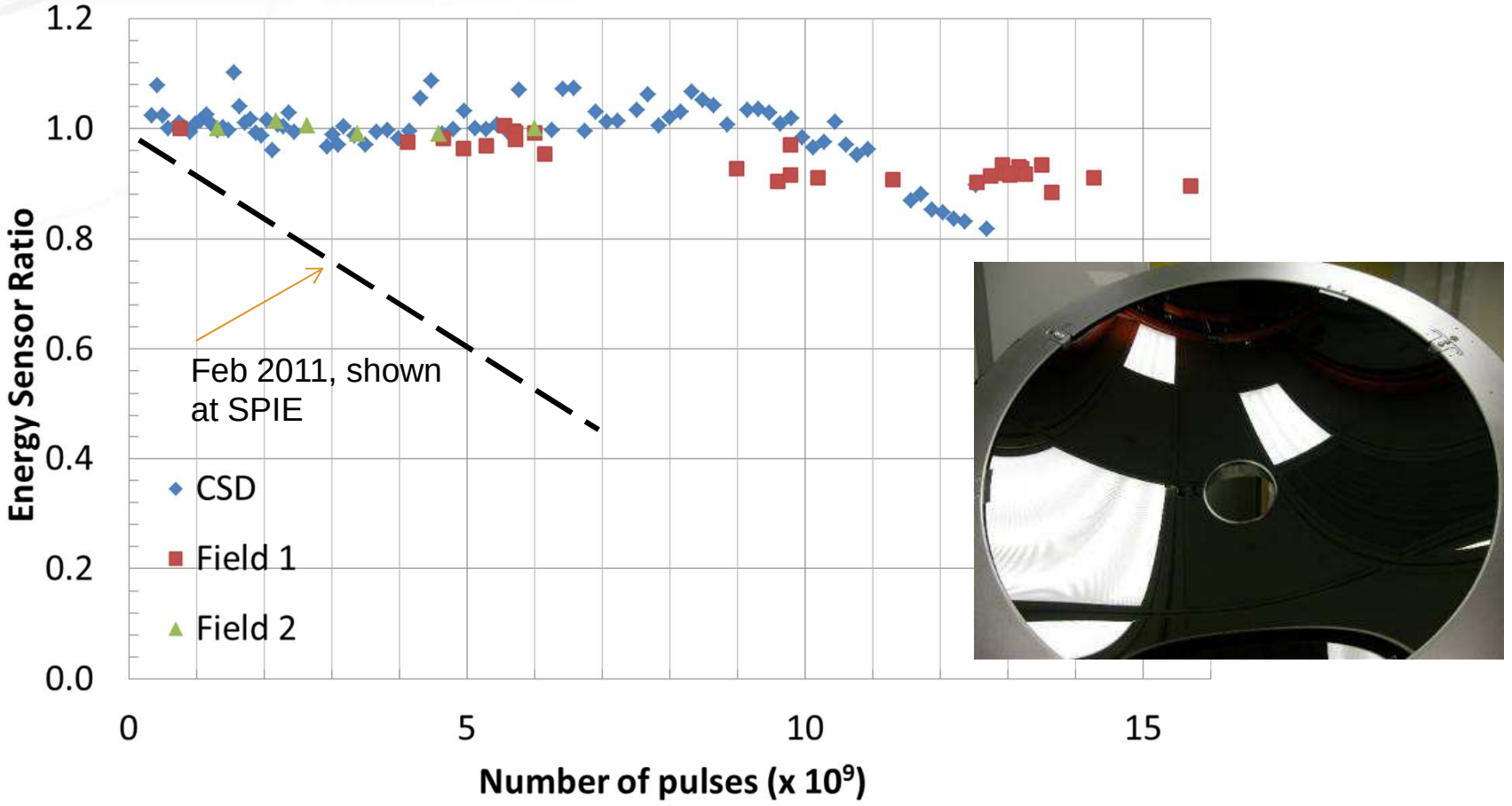
HVM I

- Prepulse hardware is installed on an internal source and ready to be tested at high duty cycle

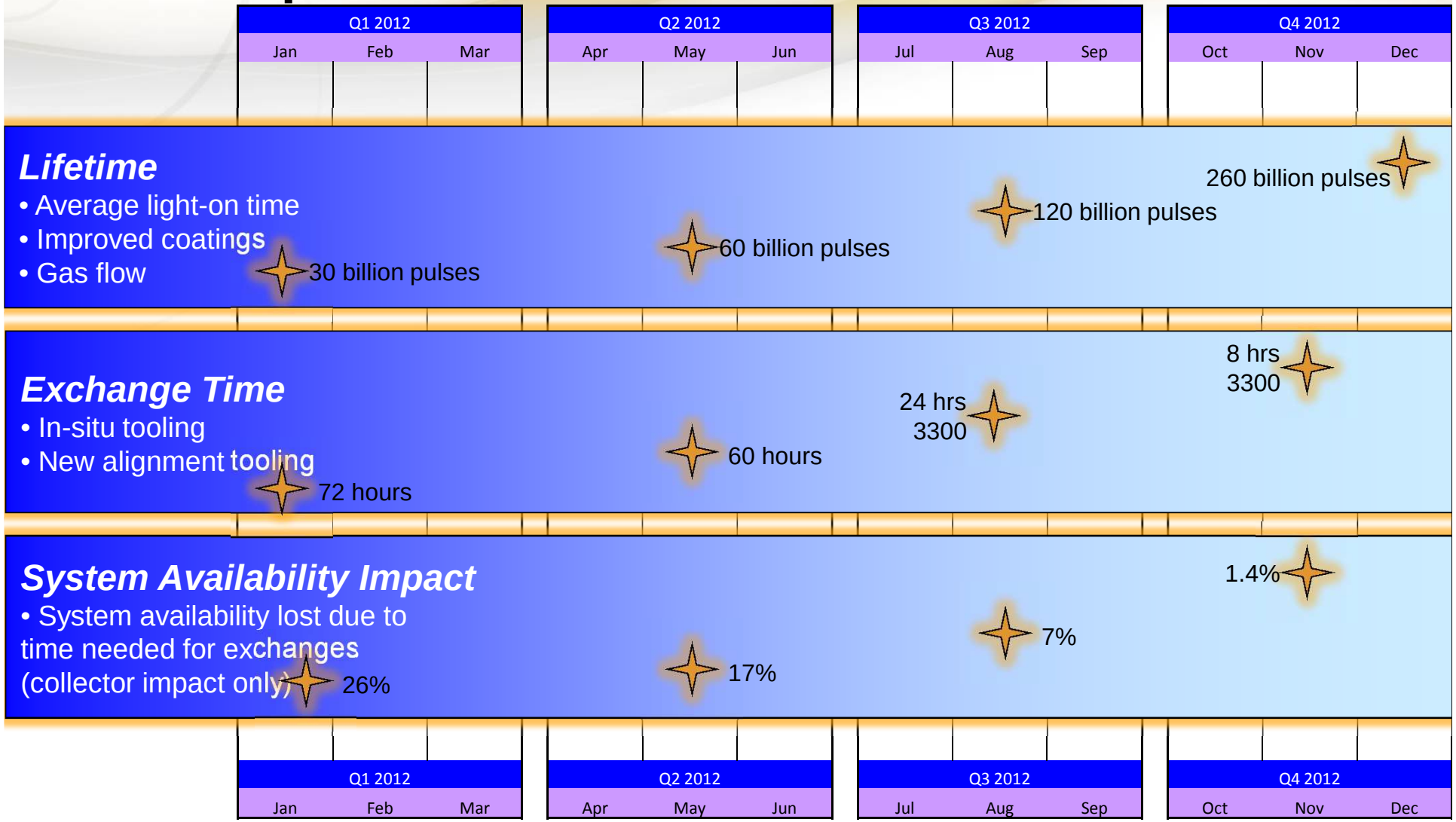


Collector Lifetime Significantly Improved since SPIE (> *16 Billion Pulses Lifetime in the Field)*

- Improvements confirmed at Cymer San Diego (CSD) and in the field
- Solutions in place to reach 30 billion pulses using improved coatings and gas flows

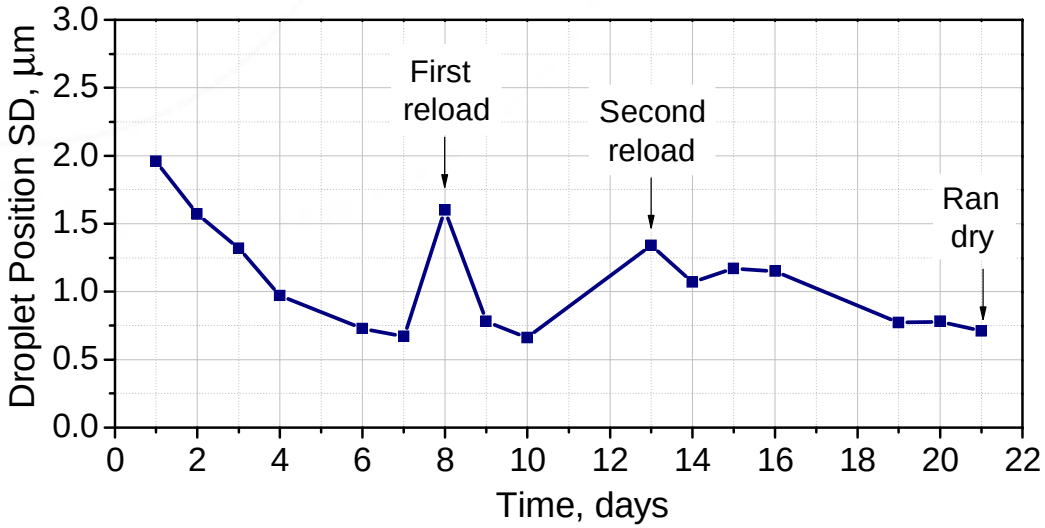


Collector Lifetime – Continuous Improvement Roadmap

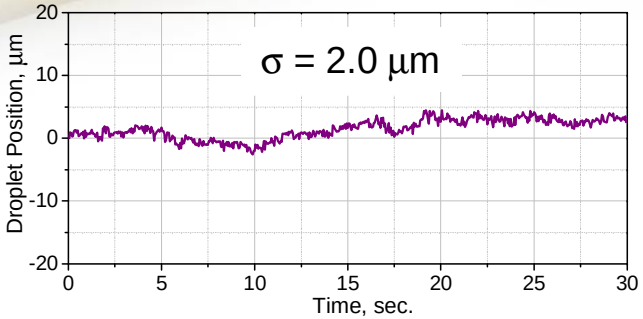


Droplet Generator: Long Term Droplet Stability over 21 days

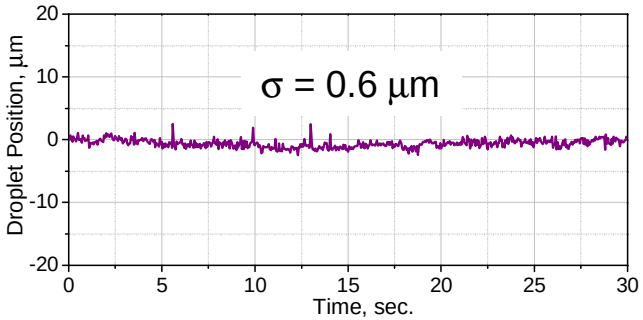
- **Standard deviation of the position stability of tin droplets measured over a period of 21 days**
- **Droplet generator was stopped for short time and refilled with tin twice during this test**



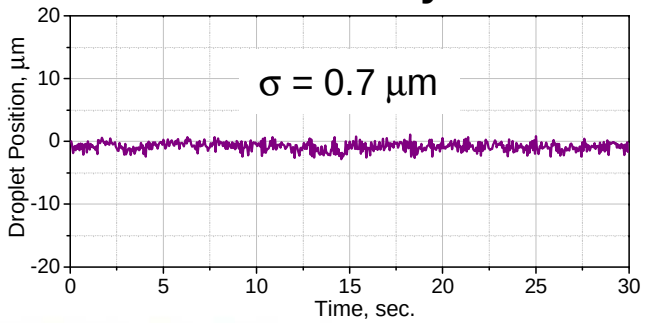
1st day



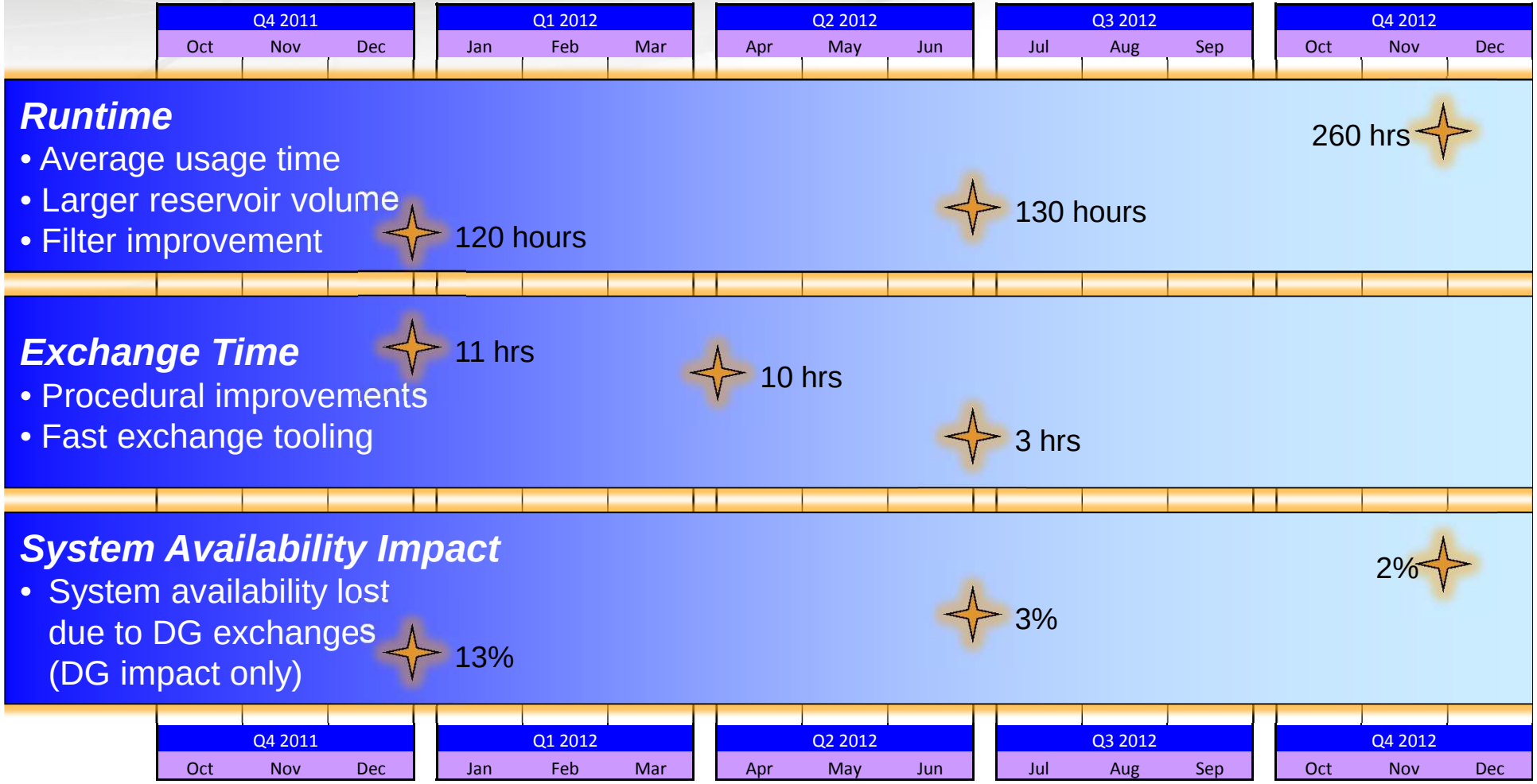
10th day



21st day



Droplet Generator – Continuous Improvement Roadmap



HVM II Development

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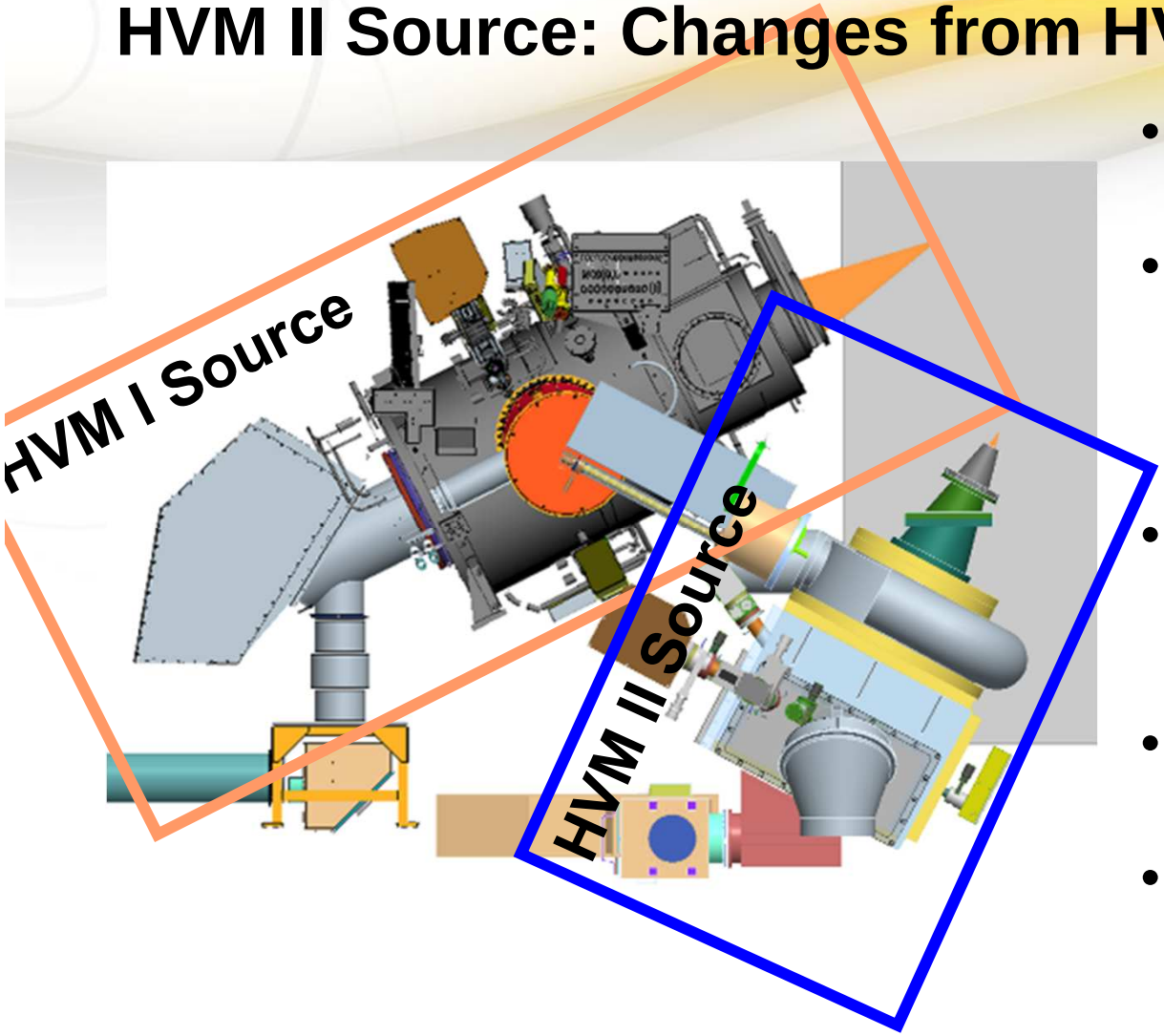
HVM II Source: Changes from HVM I



- Higher EUV Power required
- Increased source orientation angle
  - Increases scanner optical throughput
- Higher NA collector
  - Smaller source vessel
- Designed for improved serviceability
- HVM II Source architecture and layout completed, first integration begins in Q1 2012

Product Roadmap and Summary

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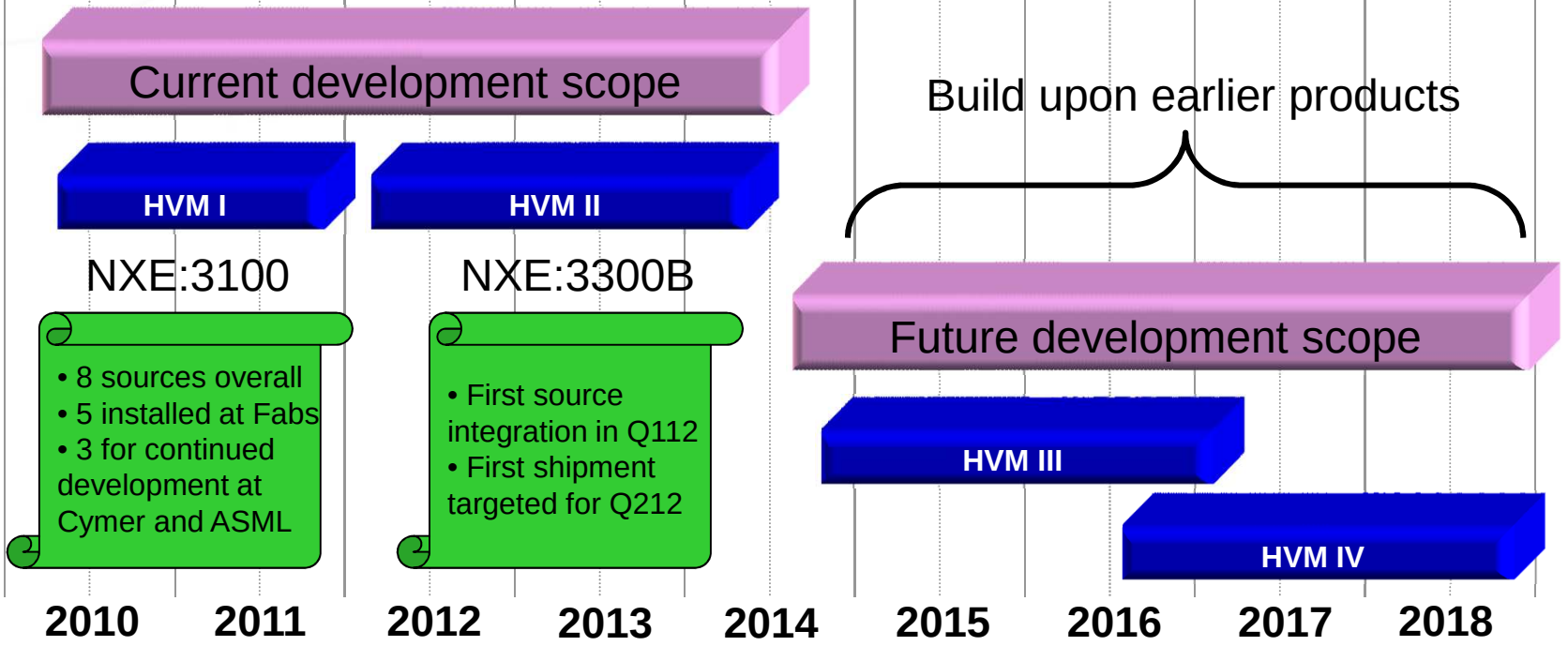
LPP EUV Source Product Roadmap

2010 2011 2012 2013 2014 2015 2016 2017 2018

EUV Source Power Roadmap				
Source Model	HVM I	HVM II	HVM III	HVM IV
Drive Laser Power (kW)	20	35	40	45
In-band CE (%)	2.5	3.0	3.5	4.0
Collection Efficiency (%)	22	26	30	33
Clean EUV Power (W)	**105**	**250**	**350**	**500**



2010 2011 2012 2013 2014 2015 2016 2017 2018

Summary

- Increased level of investment and commitment for development of LPP technology and source production for the semiconductor industry
- Eight HVM I sources built, six shipped to customers, two sources being used in San Diego for EUV power upgrades and collector protection testing
- HVM I source EUV power (clean average power) qualified at ~8W with <1.0% dose stability
- 20W clean average exposure power will be available by year end for chipmaker installations
- Exposure power as demonstrated on LT1 is >100W, validation on a HVM I source is in process to qualify upgrade 2b, with plan for chipmaker upgrade by Q2 2012
- HVM II source architecture for ASML NXE:3300B scanners is complete, modules are on order and first integration is planned in Q1 2012

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Leading the Light Generation.